Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 14 (Canceled)

Claim 15 (Currently Amended)

A System-on-Chip (SOC) apparatus, comprising:

a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals and one or more non-DMA peripherals;

a first internal unidirectional bus that couples via one or more channel controllers or caches to said one or more processor subsystems, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems and said DMA-type peripheral(s) using a Memory Access Controller and point to point unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus, said first internal unidirectional bus allows for high speed accesses to one or more shared memories between said processor subsystems and said DMA-type peripherals, said first internal unidirectional bus is optimally used for peripheral to

memory and memory to peripheral communications and can facilitate peer to peer communications;

a bus arbiter coupled to said first internal unidirectional bus, wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus; and

a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said Memory Access Controller, and said DMA-type peripheral(s), wherein said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said non-DMA peripheral(s), said Memory Access Controller, and said DMA-type peripheral(s) using point to point unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal, said second internal unidirectional bus is the communication interface between said processor subsystems and said non-DMA peripherals and provides for low speed accesses to said non-DMA peripherals;

Claim 16 (Canceled)

Claim 17 (Currently Amended)

A method that makes a System-on-Chip (SOC) apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, and one or more non-DMA peripherals;

coupling a first internal unidirectional bus via one or more channel controllers or caches to said one or more processor subsystems, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, and said DMA-type peripheral(s) using a Memory Access Controller and point to point unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus, said first internal unidirectional bus allows for high speed accesses to one or more shared memories between said processor subsystems and said DMA-type peripherals, said first internal unidirectional bus is optimally used for peripheral to memory and memory to peripheral communications and can facilitate peer to peer communications;

coupling a bus arbiter to said first internal unidirectional bus, wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus; and

providing a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said Memory Access Controller, said DMA-type peripheral(s), wherein said second internal

unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said non-DMA peripheral(s), said Memory Access Controller, said DMA-type peripheral(s) using point to point unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal, said second internal unidirectional bus is the communication interface between said processor subsystems and said non-DMA peripherals and provides for low speed accesses to said non-DMA peripherals.

Claim 18 (Currently Amended)

A method that uses a System-on-Chip (SOC) apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, and one or more non-DMA peripherals;

controlling transactions between said one or more processor subsystems and said DMA-type peripheral(s) using a first internal unidirectional bus that couples via one or more channel controllers or caches to said one or more processor subsystems, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and uses a Memory Access Controller and point to point unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts

and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus, said first internal unidirectional bus allows for high speed accesses to one or more shared memories between said processor subsystems and said DMA-type peripherals, said first internal unidirectional bus is optimally used for peripheral to memory and memory to peripheral communications and can facilitate peer to peer communications;

granting access to said first internal unidirectional bus and arbitrating memory accesses for transactions on said first internal unidirectional bus using a bus arbiter coupled to said first internal unidirectional bus; and

controlling transactions between said one or more processor subsystems, said non-DMA peripheral(s), said Memory Access Controller, and said DMA-type peripheral(s) using a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said Memory Access Controller, and said DMA-type peripheral(s), wherein said second internal unidirectional bus has a clock signal and uses point to point unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal, said second internal unidirectional bus is the

communication interface between said processor subsystems and said non-DMA peripherals and provides for low speed accesses to said non-DMA peripherals.

Claim 19 (New)

The apparatus according to claim 15 wherein said first internal unidirectional bus supports reading and writing data in bursts.

Claim 20 (New)

The apparatus according to claim 15 wherein a variable number of clock cycles elapse between any two said pipelined memory transactions.

Claim 21 (New)

The apparatus according to claim 15 wherein one or more of said DMA-type peripherals use one of the following clock signals: a clock signal having a frequency that is different from the first internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the first internal unidirectional bus clock signal, but has a different time domain than the first internal unidirectional bus clock signal.

Claim 22 (New)

The apparatus according to claim 15 wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.

Claim 23 (New)

The method according to claim 17 wherein said first internal unidirectional bus supports reading and writing data in bursts.

Claim 24 (New)

The method according to claim 17 wherein a variable number of clock cycles elapse between any two said pipelined memory transactions.

Claim 25 (New)

The method according to claim 17 wherein one or more of said DMA-type peripherals use one of the following clock signals: a clock signal having a frequency that is different from the first internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the first internal unidirectional bus clock signal, but has a different time domain than the first internal unidirectional bus clock signal.

Claim 26 (New)

The method according to claim 17 wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.

Claim 27 (New)

The method according to claim 18 wherein said first internal unidirectional bus supports reading and writing data in bursts.

Claim 28 (New)

The method according to claim 18 wherein a variable number of clock cycles elapse between any two said pipelined memory transactions.

Claim 29 (New)

The method according to claim 18 wherein one or more of said DMA-type peripherals use one of the following clock signals: a clock signal having a frequency that is different from the first internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the first internal unidirectional bus clock signal, but has a different time domain than the first internal unidirectional bus clock signal.

Claim 30 (New)

The method according to claim 18 wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.